REMARKS

Claims 2-11 and 13-19 are pending herein.

I. The allowable subject matter.

Applicants respectfully thank the Examiner for indicating the allowable subject matter. On page 21 of the January 8, 2008 Office Action, the USPTO respectfully indicates that claims 16-19 are allowed and that claims 2, 3, 8, 9, and 15 would be allowable if rewritten in independent form including all of the limitations of the base claims. Applicants respectfully accept the indicated allowable subject matter as noted in the following table, which summarizes the claim amendments:

Amended claim number	Previous claim(s) on which amended claim is based
2 (independent)	1 + 2
3 (independent)	1 + 3
8 (independent)	1 + 6 + 8
15 (independent)	12 + 15

Claims 1 and 12 have been respectfully cancelled. It is respectfully asserted that independent claims 2, 3, 8, and 15 are allowable.

II. Objections to Drawings On Page 2-4 of the Office Action.

A. The objections regarding the "first power source of claims 1, 12, and 16.

On page 2 of the Office Action, the USPTO respectfully argues that "the 'first power source' recited in claims 1, 12, and 16 must be shown or the feature(s) canceled from the claim(s)."

The Applicants respectfully note that paragraph [0036] of the present specification clarifies the first power source as shown in the Fig. 1 as follows:

> **"A control end (gate) of the correction TFT 22 is connected to a power source line PL** (voltage Pvdd), and a second conductive region (drain) is connected to a control end (gate) of a p-channel driving TFT 24"
>
> and
>
> **"...another power source line is provided to connect to the gate of the correction TFT 22..." (emphasis added)**

The Applicants respectfully note that the language of the present specification in paragraph [0036] as noted above provides clarity for the use of the term "first power source" in relation to the drawings. For example, it is respectfully asserted that the power source line PL, described above and seen in present Figure 1, is one possible example of a first power source. Thus, it is respectfully asserted that the "first power source" of claims 1, 12, and 16 is shown in the drawings.

B. The objections regarding the "four connections" of the correction transistor.

On page 2 of the present specification, the USPTO respectfully argues that "the four to the correction transistor claimed in claims 15 and 16 must be shown of the feature(s) canceled from the claim(s)."

Applicants respectfully assert that these connections are shown in present Figures 1 and 5. For example, present Figure 1 shows a correction TFT 22. As further seen in present Figure 1, the gate of correction TFT 22 is connected to power source line PL. This is one possible embodiment of the "control end connected to a first power source" claimed in claims 15 and 16, which is the first of the four connections respectfully noted by the USPTO on page 2 of the Office Action.

Additionally, present Figure 1 shows that the left terminal of correction TFT 22 is connected to the right terminal of selection TFT 20. This is one possible embodiment of the "first conductive region connected to a second conductive region of the selection transistor" claimed in claims 15 and 16, which is the second of the four connections respectfully noted by the USPTO on page 2 of the Office Action.

Also, present Figure 1 shows that the right terminal of correction TFT 22 is connected to the gate of driving TFT 24. This is one possible embodiment of the "second conductive region connected to a control end of the driving transistor" claimed in claims 15 and 16, which is the third of the four connections respectfully noted by the USPTO on page 2 of the Office Action.

Regarding the fourth connection of claim 15, i.e. "an active layer formed between the data line and the power source line to extend partially underlying at least one of these lines," Applicants respectfully note that at least one embodiment of this structure is respectfully shown in present Figure 5. Applicants respectfully note that present Figure 1 is a schematic drawing, and is therefore not suited for illustrating some of the more detailed structures of the correction TFT 22.

Accordingly, present Figure 5 shows correction TFT 22, data line DL, semiconductor layer 120, and power source line PL. As noted in paragraph [0080] of the present specification, "the region of the semiconductor layer 120 located along the data line DL forms the active layer of the correction TFT 22." As is respectfully seen in present Figure 5, this "active layer" as described in the specification is positioned between data line DL and power source line PL. Thus, it is respectfully asserted that present Figure 5 illustrates at least one possible embodiment of the "active layer formed between the data line and the power source line" of claim 15, which is the fourth connection of claim 15 respectfully noted on page 2 of the Office Action.

Regarding the fourth connection of claim 16, i.e. "at least a part of the active layer of the correction transistor is formed below the power source line with an insulating layer disposed in between," Applicants respectfully that at least one embodiment of this structure is respectfully shown in present Figure 6A.

For example, as noted above, paragraph [0080] of the specification describes the "active layer" of the correction TFT 22 is the region of semiconductor layer 120 located along data line DL. Present Figure 6A shows a cross section of a device according to claim 16 at a position where semiconductor layer 120 is located along data line DL. As further seen in

present Figure 6A, at least a part of the active layer (i.e. semiconductor layer 120) is formed below power source line PL, as claimed in claim 16. Additionally, there is a gate insulating film 104 and interlayer insulating film 106 disposed in between semiconductor layer 120 and power source line PL.

Thus, it is respectfully asserted that each of the connections of the correction transistor respectfully noted by the USPTO on page 2 of the Office Action are shown in present Figures 1, 5, and 6A.

C. The objections to Figure 13.

Applicants respectfully thank the Examiner for his suggestion and note that Figure 13 has been amended to include the legend "Prior Art," as indicated in the attached replacement sheet.

D. The objections regarding the label "SC" in the drawings.

On page 4 of the Office Action, the USPTO respectfully argues that the use of the term "SC" in the drawings is "unnecessarily confusing" because it is inconsistent with the terminology of the claims.

In response, Applicants respectfully note that paragraph [0036] of the present specification describes that a capacitor line SC functions as a pulse voltage line driven by a pulsed voltage. For example, paragraph [0036] of the present specification reads in relevant part:

> "The gate of the driving TFT 24 is also connected to one end (first electrode) of a storage capacitor 28, whose other end (second electrode) is connected to **a storage capacitor line (hereinafter referred to as a 'capacitor line' SC acting as a pulse voltage line driven by a pulsed voltage." (emphasis added)**

Thus, Applicants respectfully believe that the language of the specification in paragraph [0036] as noted above provides clarity for the use of the terms "pulse voltage line"

and "SC". Therefore, it is respectfully asserted that the use of the term "SC" in the present Figures is acceptable.

III. The objections to the specification.

On page 5 of the Office Action, the USPTO respectfully argues that the connections claimed in claim 15 are not supported by the specification. Additionally, on page 6 of the Office Action, the USPTO respectfully argues that the connections claimed in claim 16 are not supported by the specification.

A. The objections regarding claim 15.

On page 5 of the Office Action, the USPTO respectfully argues:

> "[i]n the first instance the correction transistor is not connected to the power source line but to a separate 'first power source' nor is it connected to the data line. In the second instance the correction transistor is connected to the power source line or to the data line. Such connection would require a four terminal device, which is nowhere disclosed. Further, connection of the correction transistor to the data line is nowhere disclosed but falls within the scope of the claim."

In response, Applicants respectfully note that all of the limitations described in claim 15 are clearly supported by the specification and the drawings. For example, claim 15 claims in relevant part:

> "the correction transistor includes an active layer formed between the data line and the power source line to extend partially underlying at least one of these lines."

Support for this limitation of claim 15 can be found in present Figures 5 and 11, as noted in detail above. Further support for claim 15 can be found in paragraph [0075] of the present specification. For example, paragraph [0075] of the present specification states in relevant part:

> "The correction TFT 22 connected to the selection TFT 20 is disposed so that the channel length direction thereof runs along the direction in which the data line DL extends (vertical scanning direction) in a region sandwiched by the

data line DL and the power source line PL. **The active layer of the correction TFT 22 is formed below the data line DL to underlie part of the data line DL." (emphasis added)**

Thus, Applicants respectfully believe that the above figures and specification provide sufficient proper antecedent basis for claim 15.

B. The objections regarding claim 16.

On page 6 of the Office Action, the USPTO respectfully argues:

> "[i]n the first instance the correction transistor is not connected to the power source line but to a separate 'first power source'. In the second instance the correction transistor is connected to the power source line. Such connection would require a four terminal device, which is nowhere disclosed."

In response, Applicants respectfully note that all of the limitations described in claim 16 are clearly supported by the specification and the drawings. For example, claim 16 claims in relevant part:

> "at least part of the active layer of the correction transistor is formed below the power source line with an insulating layer disposed in between."

Support for this limitation of claim 16 can be found in present Figure 6A, as noted in detail above. Further support for claim 16 can be found in paragraph [0087] of the present specification. For example, paragraph [0087] of the present specification states in relevant part:

> "As illustrated in Figs. 6A and 6B, a planarization insulating layer 108 of an organic resin or the like to planarize the upper surface is formed over the entire substrate covering the data line DL, the power source line PL, the above-described metal wiring line 24w, and the connection electrode 24e. In the planarization insulating layer 108, a contact hole is formed in a region for forming the connection electrode 24e connected to the above-described driving TFT 24. Through this contact hole, a first electrode 262 (an anode in this example) of the organic EL element 26 formed on the planarization insulating layer 108 and the connection electrode 24e are connected. When the connection electrode 24e is not provided, the first electrode 262 of the organic EL element 26 and the second conductive region 24d are directly connected by forming a contact hole penetrating the planarization insulating layer 108, the

interlayer insulating film 106, and the gate insulating film 104 in the region where the second conductive region 24d of the driving TFT 24 is formed."

Thus, Applicants respectfully believe that the above figures and specification provide sufficient proper antecedent basis for claim 16.

IV. The objections to claims 1, 12 and 16 Due To Informalities, as noted on Pages 6-7 of the Office Action.

The USPTO respectfully objects to claims 1, 12, and 16 due to informalities.

Regarding claim 1, Applicants respectfully thank the Examiner for his suggestion, which has been implemented in claims 2, 3, and 8 (which incorporated the limitations of claim 1). Thus, it is respectfully asserted that the objection has been overcome.

Regarding claims 12 and 16, Applicants respectfully thank the Examiner for his suggestions, which have been implemented in claims 15 and 16 (claim 15 was amended to include the limitations of claim 12). Thus, it is respectfully asserted that the objections have been overcome.

V. The 35 U.S.C. §112 Claim Rejections of Claims 5 and 11 as Noted on Page 7 of the Office Action.

The USPTO respectfully rejects claims 5 and 11 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5 and 11 read in relevant part:

"a scanning direction of a line-shaped pulse laser ~~irradiated~~ irradiation, when performing ~~upon~~ the polycrystallization laser annealing, onto a semiconductor layer which is an object of the polycrystallization..."

No new matter is added by the amendments. Support for the amendments is found in paragraph [0092] of the present specification and in present Figure 5.

Regarding claims 5 and 11, Applicants respectfully assert that the amendments have clarified the limitations, and therefore it is respectfully asserted that § 112 rejections of claims 5 and 11 have been overcome.

VI. The Anticipation rejections of Claims 1 and 4 based on Knapp (US 6,359,605) as Noted on Page 8 of the Office Action.

The USPTO respectfully rejects claims 1 and 4 under 35 U.S.C. 102(b) as being anticipated by Knapp. Claim 1 is an independent claim and claim 4 is a dependent claim.

Claim 1 has been respectfully cancelled. Claim 4 is now dependent on independent claim 2. As respectfully noted above, claim 2 was rewritten as an independent claim and is allowable subject matter. Therefore, it is further respectfully asserted that claim 4 is also allowable.

VII. The Obviousness Rejections of Claims 5 and 11-14 based on Knapp (US 6,359,605) in view of Kato (US 6,812,491), as Noted on Page 11 of the January 8, 2008 Office Action.

The USPTO respectfully rejects claims 5 and 11-14 under 35 U.S.C. § 103(a) as being unpatentable over Knapp in view of Kato. Claim 12 has been respectfully cancelled.

As noted above, it is respectfully asserted that independent claim 2 is allowable, and therefore it is further respectfully asserted that dependent Claim 5 is also allowable.

Additionally, as noted above, it is also respectfully asserted that independent claim 3 is allowable, and therefore it is further respectfully asserted that dependent claim 11 is also allowable.

As noted above, it is respectfully asserted that independent claim 15 is allowable, and therefore it is further respectfully asserted that dependent claims 13 and 14 are also allowable.

VIII. The Obviousness Rejections of Claims 6, 7, and 10 based on Knapp (US 6,359,605) in view of knowledge of one of ordinary skill in the art at the time of the invention as Noted on Page 11 of the Office Action.

The USPTO respectfully rejects claims 6, 7, and 10 under 35 U.S.C. § 103(a) as being unpatentable over Knapp in view of knowledge of one of ordinary skill in the art at the time of the invention. Claims 6, 7, and 10 are dependent claims.

As noted above, it is respectfully asserted that independent claim 3 is allowable, and therefore it is further respectfully asserted that dependent claims 6, 7, and 10 are also allowable.

IX. Conclusion.

Reconsideration and allowance of all of the claims is respectfully requested.

If there are any additional charges with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130.

Please contact the undersigned for any reason. Applicants seek to cooperate with the Examiner including via telephone if convenient for the Examiner.

Respectfully submitted,

By: /Daniel P. Lent/
Daniel P. Lent
Registration No. 44,867

Date: May 8, 2008
CANTOR COLBURN LLP
20 Church Street
22nd Floor
Hartford, CT 06103
Telephone (860) 286-2929
Facsimile (860) 286-0115
Customer No.: 23413